CLAIMS

What is claimed is:

1. A low loss multiple output stage of a DC-to-DC converter comprises:

first load transistor having a gate, a drain, and a source, wherein the gate of the first load transistor is operably coupled to receive a first output regulation signal, the source of the first load transistor is coupled to a first output, and the drain of the first load transistor is operably coupled to an inductor;

sink transistor having a gate, a drain, and a source, wherein the drain of the sink transistor is coupled to the drain of the first load transistor, the source of the sink transistor is coupled to a return potential, and the gate of the sink transistor is operably coupled to receive a sink output regulation signal;

second load transistor having a gate, a drain, and a source, wherein the gate of the second load transistor is operably coupled to receive a second output regulation signal, the source of the second load transistor is coupled to a second output, and the drain of the second load transistor is operably coupled to the inductor; and

gate logic module operably coupled to:

provide a voltage corresponding to the first output to the gate of the second load transistor when the first output regulation signal is active and the sink output regulation signal is inactive,

provide the second output regulation signal to the gate of the second load transistor when the second output regulation signal is active and the sink output regulation signal in inactive.

2. The low loss multiple output stage of claim 1, wherein the gate logic module further provides the voltage corresponding to the first output to a well of the second load transistor when the first output regulation signal is active and couples the well of the

second load transistor to the second output when the second output regulation signal is active.

3. The low loss multiple output stage of claim 1, wherein the gate logic module further provides a voltage corresponding to the second output voltage to the gate of the second output transistor and to a well of the second output transistor when the sink output regulation signal is active.

4. The low loss multiple output stage of claim 1 further comprises a gate oxide layer of the sink transistor being of similar thickness to the gate oxide layer of the first load transistor and a thickness of the a gate oxide layer of the second load transistor is less than thickness of the gate oxide layer of the first load transistor, wherein the first output is of a greater voltage than the second output.

5. A low loss multiple output stage of a DC-to-DC converter comprises:

first output transistor having a first on-resistance;

second output transistor having a second on-resistance, wherein the first on-resistance has a resistance value that is greater than a resistance value of the second on-resistance;

gate logic module operably coupled to the second output transistor; and

sink transistor operably coupled to allow energy to be provided to a first output via the first output transistor or to allow the energy to be provided to a second output via the gate logic module and the second output transistor based on a regulation signal, wherein voltage of the first output is greater than voltage of the second output, and wherein:

when the energy is to be provided to the first output, the gate logic module couples a gate and a well of the second output transistor to the first output,

when the sink transistor is active, the gate logic module couples the gate and the well of the second output transistor to the second output, and

when the energy is to be provided to the second output, the gate logic module couples the gate of the second output transistor to an output ground and the well of the second output transistor to the second output.

6. The low loss multiple output stage of claim 5 further comprises:

the first output transistor having a gate oxide layer thickness of a first thickness and a gate length of a first length to produce the first on-resistance; and

the second output transistor having a gate oxide layer thickness of a second thickness and a gate length of a second length to produce the second on-resistance, wherein the first thickness is greater than the second thickness and the first length is greater than the second length.

7. The low loss multiple output stage of claim 5 further comprises:

the first output having a voltage of approximately 3.3 volts; and

the second output having a voltage of approximately 1.8 volts, wherein the second on-resistance is approximately one-fourth the first on-resistance.

8. An on-chip DC-to-DC converter comprises:

a regulation module operably coupled to produce a first output regulation signal and a sink output regulation signal to regulate a first output and to produce a second output regulation signal and the sink output regulation signal to regulate a second output, wherein voltage of first output is greater than voltage of the second output;

first output capacitance operably coupled to the first output;

second output capacitance operably coupled to the second output;

an integrated circuit (IC) pad for coupling to an external inductor;

low loss output stage includes:

first load transistor having a gate, a drain, and a source, wherein the gate of the first load transistor is operably coupled to receive the first output regulation signal, the source of the first load transistor is coupled to the first output, and the drain of the first load transistor is operably coupled to the IC pad;

sink transistor having a gate, a drain, and a source, wherein the drain of the sink transistor is coupled to the source of the first load transistor, the source of the sink transistor is coupled to a return potential, and the gate of the sink transistor is operably coupled to receive a sink output regulation signal;

second load transistor having a gate, a drain, and a source, wherein the gate of the second load transistor is operably coupled to receive a second output regulation signal, the source of the second load transistor is coupled to a second output, and the drain of the second load transistor is operably coupled to the inductor; and

gate logic module operably coupled to:

provide a voltage corresponding to the first output to the gate of the second load transistor when the first output regulation signal is active and the sink output regulation signal is inactive, and

provide the second output regulation signal to the gate of the second load transistor when the second output regulation signal is active and the sink output regulation signal in inactive.

9. The on-chip DC-to-DC converter of claim 8, wherein the gate logic module further provides the voltage corresponding to the first output to a well of the second load transistor when the first output regulation signal is active and couples the well of the second load transistor to the second output when the second output regulation signal is active.

10. The on-chip DC-to-DC converter of claim 8, wherein the gate logic module further provides a voltage corresponding to the second output to the gate of the second output transistor and to a well of the second output transistor when the sink output regulation signal is active.

11. The on-chip DC-to-DC converter of claim 8 further comprises a gate oxide layer of the sink transistor being of similar thickness to the gate oxide layer of the first load transistor and a thickness of the a gate oxide layer of the second load transistor is less than thickness of the gate oxide layer of the first load transistor, wherein the first output is of a greater voltage than the second output.

12. An on-chip DC-to-DC converter comprises:

a regulation module operably coupled to produce a first output regulation signal and a sink output regulation signal to regulate a first output and to produce a second output regulation signal and the sink output regulation signal to regulate a second output, wherein voltage of first output is greater than voltage of the second output;

first output capacitance operably coupled to the first output;

second output capacitance operably coupled to the second output;

an integrated circuit (IC) pad for coupling to an external inductor;

low loss output stage includes:

first output transistor having a first on-resistance;

second output transistor having a second on-resistance, wherein the first on-resistance has a resistance value that is greater than a resistance value of the second on-resistance;

gate logic module operably coupled to the second output transistor; and

sink transistor operably coupled to allow energy to be provided to a first output via the first output transistor or to allow the energy to be provided to a second output via the gate logic module and the second output transistor based on a regulation signal, wherein voltage of the first output is greater than voltage of the second output, and wherein:

when the energy is to be provided to the first output, the gate logic module couples a gate and a well of the second output transistor to the first output,

when the sink transistor is active, the gate logic module couples the gate and the well of the second output transistor to the second output, and

when the energy is to be provided to the second output, the gate logic module couples the gate of the second output transistor to an output ground and the well of the second output transistor to the second output.

13. The on-chip DC-to-DC converter of claim 12 further comprises:

the first output transistor having a gate oxide layer thickness of a first thickness and a gate length of a first length to produce the first on-resistance; and

the second output transistor having a gate oxide layer thickness of a second thickness and a gate length of a second length to produce the second on-resistance, wherein the first thickness is greater than the second thickness and the first length is greater than the second length.

14. The on-chip DC-to-DC converter of claim 12 further comprises:

the first output having a voltage of approximately 3.3 volts; and

the second output having a voltage of approximately 1.8 volts, wherein the second on-resistance is approximately one-fourth the first on-resistance.